WHAT IS CLAIMED IS:

1. A method of processing interrupts, the method comprising:

detecting an indicator of an interrupt from a expansion device;

transferring data related to the interrupt signal from the device across the expansion bus to a local memory; and

processing the data related to the interrupt.

2. The method of claim 1, detecting an indicator of an interrupt further comprising receiving an interrupt at a central processor.

3. The method of claim 1, detecting an indicator of an interrupt further comprising receiving an interrupt on an interrupt line to a direct memory access controller.

4. The method of claim 1, detecting an indicator of an interrupt further comprising using a direct memory access controller to detect a voltage change on an interrupt line.

5. The method of claim 1, transferring data further comprising using a direct memory access controller to transfer data from any expansion devices that generated interrupt signals.

6. The method of claim 1, transferring data further comprising using a direct memory access controller to transfer data from expansion device to local memory and generating an interrupt to a central processor.

7. The method of claim 1, transferring data further comprising updating a memory access monitor bit in a memory access monitor status register.

8. A method of processing interrupts, the method comprising:

detecting interrupt signals;

determining if the interrupt signals are from local devices or expansion devices;

directing a direct memory access controller to read a status register for any expansion devices that have generated interrupt signals;

processing any interrupt signals from local devices; and

processing any interrupt signals from devices located across the bus.

9. The method of claim 8, detecting interrupt signals further comprising receiving interrupt signals at a central processor.

10. The method of claim 8, determining further comprising determining that the interrupt signals are from local devices and any expansion devices further comprise no expansion devices.

11. The method of claim 8, determining further comprising determining that the interrupt signals are from expansion devices and directing a memory access controller further comprises directing a memory access controller to process a second interrupt while processing a first interrupt.

12. A method of processing interrupts, the method comprising:

detecting an update to a descriptor memory;

updating a register corresponding to the descriptor memory in a local status register;

generating an interrupt to a central processor;

identifying a device generating the update; and

performing a task associated with the descriptor memory.

13. The method of claim 12, detecting an update to a descriptor memory further comprising detecting an update to a descriptor memory using a memory access monitor.

14. The method of claim 12, performing a task further comprising transmitting a packet.

15. The method of claim 12, performing a task further comprising determining a next hop for a received packet.

16. A method of processing interrupts, the method comprising:

detecting an interrupt at a direct memory access controller from a device located across a bus from a central processor;

transferring data from the device to a local memory; and

generating an interrupt signal to central processor when transfer is complete.

17. The method of claim 16, detecting an interrupt further comprising receiving an interrupt on an interrupt line to a direct memory access controller.

18. The method of claim 16, detecting an interrupt further comprising using a direct memory access controller to detect a voltage change on an interrupt line.

19. A device, comprising:

a central processor having at least one direct memory access controller;

an expansion bus;

at least one expansion device in communication with the central processor through the expansion bus; and

at least one interrupt signal line electrically coupled between the direct memory access controller and the expansion bus.

20. The device of claim 19, at least one interrupt signal line further comprising at least on interrupt signal line directly connected to the direct memory access controller.

21. The device of claim 19, at least one interrupt signal line further comprising a detection line electrically coupled between a central interrupt signal line and a direct memory access controller.

22. A device, comprising:

a central processor having at least one direct memory access controller;

an expansion bus;

at least one expansion device in communication with the central processor through the expansion bus; and

a memory access monitor electrically coupled to a memory to detect updates to the memory made by an expansion device.

23. The device of claim 22, the memory access monitor further to detect an update to a receive descriptor memory.

24. The device of claim 22, the memory access monitor further to detect an update to a transmission descriptor memory.

25. The device of claim 22, the memory access monitor being implemented inside a system controller.

26. The device of claim 22, the memory access monitor being implemented in software executed by a system controller.

27. An article of machine-readable media, the article containing instructions that when executed cause the machine to:

detect an indicator of an interrupt from a expansion device;

transfer data related to the interrupt signal from the device across an expansion bus to a local memory; and

process the data related to the interrupt from the local memory.

28. A device, comprising:

means for detecting an interrupt indicator from a expansion device;

means for transferring data related to the interrupt signal from the device to a local memory; and

means for processing the data related to the interrupt.

29. An article of machine-readable media, the article containing instructions that when executed cause the machine to:

detect interrupt signals;

determine if the interrupt signals are from local devices or expansion devices;

direct a direct memory access controller to read a status register for any expansion devices that have generated interrupt signals;

process any interrupt signals from local devices; and

process any interrupt signals from devices located across the bus.

30. A device, comprising:

means for detecting interrupt signals;

means for determining sources of the interrupt signals;

means for directing a direct memory access controller to read a status register for any expansion devices that have generated interrupt signals;

means for processing any interrupt signals from local devices; and

processing any interrupt signals from expansion devices.

31. An article of machine-readable media, the article containing instructions that when executed cause the machine to:

detect an update to a descriptor memory;

update a register corresponding to the descriptor memory in a local status register;

generate an interrupt to a central processor;

identify a device generating the update; and

perform a task associated with the descriptor memory.

32. A device, comprising:

means for detecting an update to a descriptor memory;

means for updating a register corresponding to the descriptor memory in a local status register;

means for interrupting a central processor;

means for identifying a device generating the update; and

means for performing a task associated with the update.

33. A device, comprising:

means for detecting an interrupt at a direct memory access controller from an expansion device;

means for transferring data from the device to a local memory; and

means generating an interrupt signal to central processor when transfer is complete.